

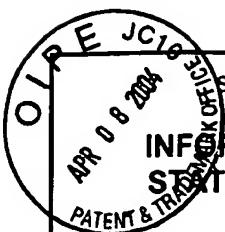
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet	1	of	2	Attorney Docket Number	SPLX.P0091
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U.S. PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ⁴ (if known)			
	1. 2002/0157 063		A1	10-24-2002	Besson	
	2. 2002/0178 432		A1	11-28-2002	Kim et al.	
	3. 2003/0145 288		A1	07-31-2003	Wang et al.	
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	13. 6,311,317		B1	10-30-2001	Khoche et al.	
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18-MARCH-2005

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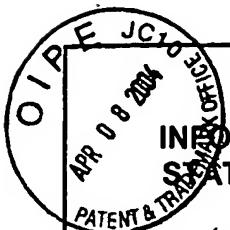
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STATEMENT BY APPLICANT**
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Sheet 2 of 2					Application Number 10/061,459
					Filing Date 1/31/02
					First Named Inventor Steven Teig, et al.
					Group Art Unit 2825
					Examiner Name Thompson, Annette
					Attorney Docket Number SPLX.P0091

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	21.	6,519,609	B1	02-11-2003	Touzet	
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	25.	6,546,541	B1	04-08-2003	Petranovic et al.	
	26.	6,618,835	B1	09-09-2003	Garlapati et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					T ⁵
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	29.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargetting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics", Vol. 2, 14 May 2000, pp. 703-706.					
	30.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.					
	31.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.					
	32.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 th Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.					

Examiner Signature	Date Considered	18-MARCH-2005
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	SPLX.P0091

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	1.	5,311,442		05-10-1994	Fukushima	
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	10.	6,473,884		10-29-2002	Ganai et al	
	11.	6,490,717		12-03-2002	Pedersen et al	
	12.	6,546,539		04-08-2003	Lu et al	

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	1.	5,519,630		05-21-1996	Nishiyama et al.	
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	7.	6,301,696	B1	11-09-2001	Lien et al.	

NON PATENT LITERATURE DOCUMENTS

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	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
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